

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Dave Goh, et al.

Confirmation No.: 1530

Application No.: 09/102,207

Examiner: David D. Davis

Filing Date: June 22, 1998

Group Art Unit: 2652

Title: WEB SERVER CHIP FOR NETWORK MANAGEABILITY

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on April 2, 2005.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) \$500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

() (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

() one month	\$120.00
() two months	\$450.00
() three months	\$1020.00
() four months	\$1590.00

() The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of \$500.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit: April 30, 2005

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Respectfully submitted,

Dave Goh, et al.

By Douglas L. Weller

Douglas L. Weller

Attorney/Agent for Applicant(s)

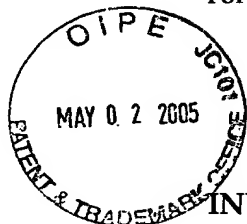
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PATENT APPLICATION
ATTORNEY DOCKET NO.10971798-1



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EXAMINER: David Donald Davis

SUBJECT: WEB SERVER CHIP FOR NETWORK MANAGEABILITY

COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, VA 22313-1450

SIR:

APPEAL BRIEF

Appellant herein sets forth his reasons and arguments for appealing the Examiner's final rejection of claims in the above-identified case.

REAL PARTY IN INTEREST

This Patent Application has been assigned to Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas.

RELATED APPEALS AND INTERFERENCES

Appellant is aware of no related appeals or interferences.

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STATUS OF CLAIMS

Claims 1 through 41 are extant in the case.

Claims 31 through 41 have been withdrawn from consideration.

Claims 1 through 30 are rejected.

The appealed claims are claims 1 through 30.

STATUS OF AMENDMENTS

After the final rejection, Appellant filed a Response to Office Action dated February 16, 2005. In the Response to Office Action, no amendments were made to the claims.

SUMMARY OF THE INVENTION

Network management typically includes monitoring and controlling resources in computers. However, software for performing network management can be expensive to purchase and maintain. Agents within the network management use precious computational resources burdening a host computer. See the Specification at page 1, lines 6 through 31.

In one embodiment of the present invention, network management is accomplished with the use of a chip (38) for incorporation within a network device (18) that is connectable to a computer network (20,24,34). The network device (18) includes a host processor (40). See Figure 1 and the Specification at page 4, line 18 through page 5, line 2.

The chip (38) includes a media access controller (42), a host interface (52-54) and an embedded processor (48). The media access controller (42) is connectable to the computer network (20,24,34). The media access controller (42) provides the chip (38) with access to the computer network (20,24,34) independent of the host processor (40). See Figure 3 and the Specification at page 7, line 23 through page 8, line 10.

The host interface (52-54) is connectable to the host processor (40). See Figure 3, and the Specification at page 8, line 22 through page 10 line 4.

The embedded processor (48) is coupled between the host interface (52-54) and the media access controller (42). The embedded processor (48) is programmable to function as a manageability web server, communicate with the host interface (52-54) and obtain manageability information about the network device (18). The embedded processor (48) is also programmable to send the manageability information to the media access controller (42) for transmission over the computer network (20,24,34). In this way, the chip (38) performs network management functions independent of the host processor (40). See Figure 3 and the Specification at page 11, line 12 through page 12, line 3.

For example, the network device (18) includes interchip communications means (70), a compliant device (74), a chip (38) and non-volatile memory (68). The compliant device (74) is coupled to the interchip communications means (70). See Figure 3 and the Specification at page 12, line 24 through page 13, line 5.

For example, the embedded processor (48) is coupled to the media access controller (42) and programmed to function as an HTTP manageability web server. See the Specification at page 12, lines 4 through 12.

The network manager (30) is coupled to the computer network (20,24,34). The network manager (30) includes a web browser and a plurality of HTML files for instructing the network manager (30) to communicate with the embedded processor (48) in the network device (18) and perform network management of the network device (18). In this way, the embedded processor (48) can communicate with the network manager (30) independent of the host processor (40). See the Specification at page 11, lines 12 through 23.

ISSUES PRESENTED FOR REVIEW

The following issues are presented for review:

(1) whether under 35 U.S.C. § 102 (e) claims 1 through 3, 5, 6, 8, 12 through 15, and 19 through 20 are anticipated by USPN 6,532,497 (*Cromer*).

(2) whether under 35 U.S.C. § 103 (a) claims 7, 9 through 11, 18 and 21 through 30 are patentable over *Cromer*.

(3) whether under 35 U.S.C. § 103 (a) claims 4, 16 and 17 are patentable over *Cromer* in view of USPN 5,903,737 (*Han*).

GROUPING OF CLAIMS

The claims (1 through 3, 5, 6, 8, 12 through 15, and 19 through 20) rejected under 35 U.S.C. § 102(e) do not stand or fall together. The claims 1 through 3, 5, 6, 8, 12 through 15, and 19 through 20 are divided into two groups. The first group contains claims 1 through 3 and 5, 8 and 12. The second group contains claims 13 through 15 and 19 through 20.

In the argument section below, Appellant points out why the claims of each group are separately patentable. In short, each of the groups includes an independent claim that sets out a different combination of elements than the independent claims in the other groups. Each of the independent claims sets out subject matter that is patentable over the cited art. Each group of claims is therefore separately patentable over the cited prior art.

ARGUMENT

Rejection of Claims under 35 U.S.C. § 102(e)

A. Overview specifying errors in the rejection of the claims.

The criteria for a rejection under 35 U.S.C. § 102 has been clearly defined by the courts and confirmed by the U.S. Patent and Trademark Office. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Examiner has failed to show that each and every element set forth in the claims is found either expressly or inherently in *Cromer*.

Below, Appellant clearly and unambiguously points out subject matter within each independent claim that is not disclosed or suggested by *Cromer*. On the basis of this, Appellant believes all the claims are patentable over *Cromer*.

B. Description of *Cromer*.

Cromer discloses a separately powered network interface for reporting the activity states of a network connected client.

Figure 5 of *Cromer* shows an implementation of logic 400, used to collect selected system information. See *Cromer* at column 1, lines 35 through 38. The logic 400 monitors logic signals from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304. See *Cromer* at column 3, lines 44 through 47.

Within logic 400 a non-volatile memory 504 is shown. The non-volatile memory 504 is used to store information for packet generation such as IP header, UDP header and universal identifier (UUID). See *Cromer* at column 3, lines 55 through 59.

C. Discussion of group 1 claims (claims 1 through 3, 5, 6, 8, 12).

1. Subject matter within independent claim 1 not disclosed by *Cromer*.

Independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access

controller, a host interface and an embedded processor. The embedded processor is between the host interface and the media access controller. The embedded processor is programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network.

Cromer does not disclose or suggest an embedded processor being programmable to function as a manageability web server, as set out in claim 1.

Cromer does not disclose or suggest an embedded processor being programmable to send manageability information to a media access controller for transmission over the computer network, as set out in claim 1.

2. Errors made by the Examiner in the stated rationale for the rejection.

The Examiner has failed to correctly ascertain the disclosed subject matter of *Cromer*. This has led to an incorrect rejection of independent claim 1 over *Cromer*. Below, Appellant specifically responds to incorrect assertions made by the Examiner pertaining to the disclosed subject matter in *Cromer*.

a. Response to the Examiner's argument that in *Cromer* the logic 400 is programmable to function as a manageability web server.

The Examiner has asserted: "*Cromer* et al discloses in column 3, lines 32-52 that the embedded processor 400 is programmable to function as a

manageability web server..." See the Office Action *mailed* January 12, 2005 at page 3, lines 5 through 7. This statement by the Examiner is incorrect.

Cromer at column 3, lines 44 through 47 states the following:

The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 detects states, creates packets, and sends data over the MII bus to physical layer 304. This is the only functionality that *Cromer* discloses that is performed by logic 400. Nowhere does *Cromer* disclose or suggest that logic 400 is programmed to function as a manageability web server. In fact, nowhere does *Cromer* indicate that logic 400 is able to receive packets or any other communications over a network. Thus, it is clear that *Cromer* does not disclose or suggest logic is programmed to function as a manageability web server.

b. Response to the Examiner's argument that in *Cromer* the logic 400 is programmable to send manageability information to the media access controller 308 for transmission over the computer network.

The Examiner has asserted: "The embedded processor 400 further is programmable to send the manageability information to the media access controller 308 for transmission over the computer network." See the Office Action *mailed* January 12, 2005 at page 3, lines 7 through 9. This assertion by the Examiner is incorrect and has no foundation in the subject matter actually disclosed by *Cromer*.

For example, *Cromer* at column 3, lines 42 through 47 states the following:

By so connecting the logic 400 at the MII bus, it can send network packets using the physical layer 304. The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 sends data to physical layer 304, not to the media access controller 308. While logic 400 and media access controller 308 are both connected to the MII bus, nowhere does *Cromer* give any disclosure or suggestion that logic 400 and media access controller ever communicate with each other.

There is therefore no disclosure or suggestion in *Cromer* that logic 400 is programmable to send manageability information to the media access controller 308 for transmission over the computer network. The Examiner's assertion to the contrary has no foundation in the subject matter actually disclosed by *Cromer*.

D. Discussion of group 2 claims (claims 13 through 15, 19 and 20).

1. Subject matter within independent claim 13 not disclosed by *Cromer*.

Independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and an embedded processor. Non-volatile memory is programmed with a plurality of executable instructions. The instructions, when executed, instructs the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and

send the manageability information to the media access controller for transmission over the computer network.

Cromer does not disclose or suggest a non-volatile memory programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to function as a manageability web server, and send manageability information to a media access controller for transmission over the computer network.

2. Errors made by the Examiner in the stated rationale for the rejection.

The Examiner has failed to correctly ascertain the disclosed subject matter of *Cromer*. This has led to an incorrect rejection of independent claim 13 over *Cromer*. Below, Appellant specifically responds to incorrect assertions made by the Examiner pertaining to the disclosed subject matter in *Cromer*.

a. Response to the Examiner's argument that in *Cromer* non volatile memory 504 is programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to function as a manageability web server.

The Examiner has asserted the following:

Figure 5, in particular, of *Cromer* et al shows non-volatile memory programmed with a plurality of executable instructions (source, destination, length, etc.). The instructions, when executed, instructing the embedded processor 400 to function as a manageability web server, communicate with the interchip communication to obtain manageability information about the compliant device and send the manageability information to the media access controller 308 for transmission over the computer network.

See the Office Action *mailed* January 12, 2005 at page 4, lines 7 through

9. The assertion by the Examiner that non volatile memory 504 is

programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to function as a manageability web server is clearly incorrect and has no basis in the disclosure or teaching of *Cromer*.

Cromer at column 3, lines 55 through 59 states the following:

When timer 508 expires, microcontroller 502 according to the invention will gather information for packet generation such as IP header, UDP header and universal identifier (UUID) from non-volatile memory 504.

This is the only information *Cromer* discloses about non-volatile memory 504. Nothing in *Cromer* discloses or suggests that non-volatile memory is programmed with a plurality of executable instructions, the instructions, when executed, instructing an embedded processor to function as a manageability web server, as set out in claim 13 of the present case.

b. Response to the Examiner's argument that in *Cromer* non volatile memory 504 is programmed with a plurality of executable instructions that, when executed, instructs an embedded processor to send manageability information to a media access controller for transmission over a computer network.

The Examiner has asserted the following:

Figure 5, in particular, of *Cromer* et al shows non-volatile memory programmed with a plurality of executable instructions (source, destination, length, etc.). The instructions, when executed, instructing the embedded processor 400 to ... send the manageability information to the media access controller 308 for transmission over the computer network.

See the Office Action *mailed* January 12, 2005 at page 4, lines 7 through

9. This assertion by the Examiner is incorrect and has no foundation in the subject matter actually disclosed by *Cromer*.

For example, *Cromer* at column 3, lines 42 through 47 states the following:

By so connecting the logic 400 at the MII bus, it can send network packets using the physical layer 304. The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 sends data to physical layer 304, not to the media access controller 308. While logic 400 and media access controller 308 are both connected to the MII bus, nowhere does *Cromer* give any disclosure or suggestion that logic 400 and media access controller ever communicate with each other. This is a clear teaching away from the subject matter set out in claim 1 of the present case.

Rejection of Claims under 35 U.S.C. § 103(a)

A. Overview Specifying Errors in the Rejection of the Claims.

The U.S. Patent and Trademark Office has set forth a methodology for establishing a *prima facie* case of obviousness. Specifically three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

See MPEP 706.02 (j).

Appellant believes the Examiner has failed to establish a *prima facie* case of obviousness for the claims extant in the present case because there are claim limitations that are not taught or suggested by *Cromer* and/or *Han*.

B. Discussion of claims 7, 9 through 11, 18 and 21 through 30 rejected as unpatentable over *Cromer*.

Appellant believes the Examiner has failed to establish a *prima facie* case of obviousness for claims 7, 9 through 11, 18 and 21 through 30 because there are claim limitations in each of these claims that are not taught or suggested by *Cromer*.

1. Subject matter within independent claim 23 not disclosed by *Cromer*.

Independent claim 23 sets out a system. The system includes a network device. The network device includes a chip. The chip includes a media access controller and an embedded processor programmed to function as an HTTP manageability web server. *Cromer* does not disclose or suggest a chip including an embedded processor programmed to function as an HTTP manageability web server.

a. Response to the Examiner's argument that in *Cromer* the logic 400 can be programmed to function as a manageability web server.

The Examiner has asserted the following: "In column 1, lines 40 through 44 of *Cromer* et al discloses that processor 400 can be programmed to function as a manageability web server and a network manager coupled to the computer network." See the Office Action mailed January 12, 2005, at

page 6, lines 7 through 9. This statement by the Examiner is incorrect. In column 1, lines 40 through 44, *Cromer* discusses prior art software available to manage systems remotely. In column 1, lines 40 through 44, *Cromer* is not discussing logic 400. Nothing in column 1, lines 40 through 44 can be interpreted as disclosing or suggesting that logic 400 is programmed to function as an HTTP manageability web server.

Cromer at column 3, lines 44 through 47 states the following:

The logic 400 according to the invention monitors logic signal from client system 104, detects states, creates packets, and sends data over the MII bus to physical layer 304.

Cromer thus specifically teaches that logic 400 detects states, creates packets, and sends data over the MII bus to physical layer 304. This is the only functionality that *Cromer* discloses that is performed by logic 400. Nowhere does *Cromer* disclose or suggest that logic 400 is programmed to function as an HTTP manageability web server. In fact, nowhere does *Cromer* indicate that logic 400 is able to receive packets or any other communications over a network. Thus it is clear that *Cromer* does not disclose or suggest logic 400 is programmed to function as an HTTP manageability web server.

2. Discussion of dependent claims 7, 9 through 11, 18, 21, 22 and 24 through 30.

Claims 7, 9 through 11, 18, 21, 22 and 24 through 30 are patentable based on the patentability of their underlying independent claims.

C. Discussion of claims 4, 16 and 17 rejected as unpatentable over *Cromer* in view of *Han*.

Appellant believes the Examiner has failed to establish a *prima facie* case of obviousness for claims 4, 16 and 17 because there are claim limitations in each of these claims that are not taught or suggested by *Cromer* and/or *Han*.

1. Description of *Han*.

Han discloses an apparatus and method for serial data communication utilizing general microcomputer.

2. Discussion of claims 4, 16 and 17.

Claims 4, 16 and 17 are patentable based on the patentability of the underlying independent claims. *Han* does not disclose or suggest the information lacking from *Cromer*.

a. Discussion of dependent claim 4.

Claim 4 is patentable over *Cromer* and *Han* based on the subject matter set out in independent claim 1. As discussed above, independent claim 1 sets out a chip for incorporation within a network device connectable to a computer network. The chip includes a media access controller, a host interface and an embedded processor. Neither *Cromer* nor *Han* disclose an embedded processor as described in claim 1 of the present case.

Specifically, claim 1 sets out that an embedded processor is between the host interface and the media access controller. The embedded processor is

programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device. The embedded processor further is programmable to send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by *Cromer* or *Han*.

b. Discussion of dependent claims 16 and 17.

Claims 16 and 17 are patentable over *Cromer* and *Han* based on the subject matter set out in independent claim 13. As discussed above, independent claim 13 sets out a network device. The network device includes a chip. The chip includes a media access controller, an interchip communications interface and an embedded processor. The embedded processor is not disclosed or suggested by *Cromer* or *Han*.

Non-volatile memory is programmed with a plurality of executable instructions. The instructions, when executed, instructs the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network. None of this functionality is disclosed or suggested by *Cromer* or *Han*.

CONCLUSION

For all the reasons discussed above, Appellant believes the rejection of the claims was in error and respectfully requests that the rejection be reversed.

Respectfully submitted,
DAVE GOH, ET AL.

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Appendix: Appealed Claims

1. A chip for incorporation within a network device connectable to a computer network, the network device including a host processor, the chip comprising:

a media access controller connectable to the computer network, the media access controller providing the chip with access to the computer network independent of the host processor;

a host interface connectable to the host processor; and

an embedded processor coupled between the host interface and the media access controller;

the embedded processor being programmable to function as a manageability web server, communicate with the host interface and obtain manageability information about the network device;

the embedded processor further being programmable to send the manageability information to the media access controller for transmission over the computer network;

whereby the chip performs network management functions independent of the host processor.

2. The chip of claim 1, wherein the embedded processor is programmable to obtain the manageability information in response to a network request addressed to the manageability web server.

3. The chip of claim 1, the network device further including an interchip communications means and a compliant device coupled to the interchip communication means, wherein the chip includes an interface connectable to the interchip communications means, and wherein the embedded processor is programmable to communicate via the interchip communication means interface to obtain manageability information about the compliant device.

4. The chip of claim 3, wherein the interchip communication means includes an I²C bus, and wherein the compliant device is an I²C-compliant device.

5. The chip of claim 3, wherein the embedded processor is also programmable to control the compliant device coupled to the interchip communications means.

6. The chip of claim 5, wherein the compliant device is a power supply controller, and wherein the embedded processor is programmable to control the power supply controller.

7. The chip of claim 5, wherein the compliant device is a fan controller, and wherein the embedded processor is programmable to control the fan controller.

8. The chip of claim 5, wherein the embedded processor is programmable to control the compliant device in response to a network request addressed to the manageability web server.

9. The chip of claim 5, wherein the embedded processor is programmable to perform firmware upgrades of the network device.

10. The chip of claim 1, wherein the embedded processor is programmable to perform network communications using TCP/IP.

11. The chip of claim 1, wherein the embedded processor is programmable to implement an HTTP web server.

12. The chip of claim 1, wherein the embedded processor is programmable to obtain manageability information from the host processor.

13. A network device connectable to a computer network, the network device comprising:

interchip communications means;

a compliant device coupled to the interchip communications means;

a chip including a media access controller connectable to the computer network; an interchip communications interface connected to the interchip communications means; and an embedded processor coupled to the interchip communications interface and the media access controller; and non-volatile memory programmed with a plurality of executable instructions, the instructions, when executed, instructing the embedded processor to function as a manageability web server, communicate with the interchip communications means to obtain manageability information about the compliant device, and send the manageability information to the media access controller for transmission over the computer network.

14. The network device of claim 13, wherein the instructions instructs the embedded processor to obtain the manageability information from the compliant device in response to network requests addressed to the manageability web server.

15. The network device of claim 13, further comprising a host processor; wherein the chip includes a host interface coupled to the host processor and the embedded processor, and wherein the instructions instruct the embedded processor to obtain manageability information from the host processor.

16. The network device of claim 13, wherein the interchip communications means includes an I²C bus, wherein the compliant device is an I²C-compliant device, and wherein the instructions instruct the embedded processor to control the I²C-compliant device in response to network requests addressed to the manageability web server.

17. The network device of claim 16, wherein the I²C-compliant device is a power supply controller, and wherein the instructions instruct the embedded processor to control the power supply controller,

18. The network device of claim 16, wherein the I²C-compliant device is a fan controller, and wherein the instructions instruct the embedded processor to control the fan controller.

19. The device of claim 13, wherein the non-volatile memory further stores web page content.

20. The device of claim 13, further comprising volatile memory for storing the manageability information.

21. The device of claim 13, wherein the instructions instruct the embedded processor to perform network communications using TCP/IP.

22. The device of claim 13, wherein the instructions instruct the embedded processor to implement an HTTP web server.

23. (Previously presented) A system comprising:

a computer network;

a network device including a host processor and a chip, the chip including

a media access controller coupled to the computer network, and

an embedded processor coupled to the media access controller and programmed to function as an HTTP manageability web server; and

a network manager coupled to the computer network, the network manager including a web browser and a plurality of HTML files for instructing the network manager to communicate with the embedded processor in the network device and perform network management of the network device;

whereby the embedded processor can communicate with the network manager independent of the host processor.

24. The system of claim 23, wherein the network device includes a compliant device and wherein the embedded processor is programmable to control the compliant device in response to control requests from the network manager.

25. The system of claim 24, wherein the compliant device is a fan controller, and wherein the network manager can request the embedded processor to control the fan controller to adjust fan speed.

26. The system of claim 24, wherein the compliant device is a power supply controller, and wherein the network manager can request the embedded processor to control the power supply controller to shut down and turn on the network device at scheduled times.

27. The system of claim 24, wherein the compliant device is a power supply controller, and wherein the network manager can request the embedded processor to control the power supply controller to reboot the computer.

28. The system of claim 24, wherein the network device further includes an upgradable BIOS; and wherein the network manager can send a BIOS upgrade program to the embedded processor and request the embedded processor to run the BIOS upgrade program.

29. The system of claim 24, wherein the network manager can send a diagnostic program to the embedded processor and request the embedded processor to run the diagnostic program and return to the network manager results obtained by the diagnostic program.

30. The system of claim 23, wherein the embedded processor is programmable to communicate with host interface and obtain manageability information from the host processor in response to requests by the network manager.